What is claimed is:

1. A data output buffer having a preset structure, comprising:

a plurality of groups, each group having two data output buffers;

a preset driver for precharging or discharging any one output of two output buffers in each group;

a control circuit for generating a control signal to drive the preset driver when outputs of the two output buffers in each group are same; and

a set circuit connected between the outputs of the two data output buffers in each group, for making the outputs of the two data output buffer in each group the same level.

2. The data output buffer having a preset structure as claimed in claim 1, wherein the preset driver comprises:

a first switching device for precharging a selected output of the two data output buffers in each group with Vcc according to a first driving signal; and

a second switching device for discharging the selected output according to a second driving signal.

3. The data output buffer having a preset structure as claimed in claim 1, wherein the control circuit comprises:

an evaluation circuit for generating a preset signal and a preset enable signal depending on whether the outputs of the two data output buffers in each group are same; and

a preset circuit for generating the first driving signal and the second driving signal according to a preset signal and a preset enable signal of the evaluation circuit.

4. The data output buffer having a preset structure as claimed in claim 1, wherein the set circuit comprises a third switching device for connecting the outputs of the two data output buffers in each group before the two data output buffers each group output effective data.

5. The data output buffer having a preset structure as claimed in claim 3, wherein the evaluation circuit comprises:

a first switching device for switching any one output of the two data buffers in each group according to a first control signal;

a first latch for latching the output of the first switching device;

a second switching device for switching a remaining output the two data buffers in each group according to the first control signal;

a second latch for latching the output of the second switching device;

a first NOR gate for performing a NOR operation on the outputs of the first and second latches;

a first NAND gate for performing a NAND operation on the outputs of the first and second latches;

a first inverter for inverting the output of the first NAND gate;

a second inverter for inverting the output of the first inverter to generate a preset signal;

a second NOR gate for performing a NOR operation on the output of the first NOR gate and the output of the first inverter;

a second NAND gate for performing a NAND operation on an inverted signal of the second NOR gate, an inverted first control signal and a delayed first control signal to generate a preset enable signal.

6. The data output buffer having a preset structure as claimed in claim 3, wherein the preset circuit comprises:

a NOR gate for performing a NOR operation on the preset enable signal and the third control signal;

a first inverter for inverting the output of the NOR gate;

a first switching device that is turned on according to the output of the NOR gate and the output of the first inverter;

a second switching device that is turned on according to the output of the NOR gate and the output of the first inverter;

a third switching device that is switched according to the output of the NOR gate, thereby making the preset signal the first driving signal; and

a fourth switching device that is switched according to the output of the first inverter, thereby making the preset signal the second driving signal.